Remarks

Independent claim 1 describes a method of forming an electronic device comprising the following steps.

First, the method provides an inner semiconductor substrate. On the outer surface of the inner substrate, the method forms a buried conductive layer. On the outer surface of the buried layer, the method forms a semiconductive bonding layer. And to outer surface of the bonding layer the method bonds an outer substrate. The outer substrate comprises a buried insulator layer that has a surface, which bonds to the bonding layer. The outer substrate further comprises a semiconductive device layer.

In the Office action dated January 15, 2003, the examiner rejected claim 1 as unpatentable under 35 U.S.C. 103(a) over Knodo et al. (U.s. 5,536,361) in view of Ohmi et al. (6,255,731 B1). However, the Office action failed to establish *prima facie* obviousness for the following reasons.

1. **Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination.**

The Kondo reference teaches a process for preparing a semiconductor substrate, which comprises a step of making a silicon mono-crystalline layer on the resulting porous substrate, a step of bonding the surface of the non-porous silicon mono-crystalline layer to another substrate having a metallic surface, and a step of removing the porous silicon layer of the bonded substrates by selective etching.[1]

The Ohmi reference teaches the forming of a semiconductor substrate by causing two metals, a metal and a semiconductor, a metal and a metal-semiconductor compound, a semiconductor and a metal-semiconductor compound, or two metal-semiconductor compounds to react with each other. The result of the reaction is a structure that

[1] See U.S. 5,536,361, Abstract.

comprises a support, an electroconductive material layer, an insulating layer, and a semiconductor layer arranged sequentially in the above order.[2]

There are seven examples in the Kondo reference and six examples in the Ohmi reference. Not one example teaches the process of claim 1 of the present invention. The inner substrate described in claim 1 has a conductive layer formed on a semiconductor substrate and a semiconductor bonding layer formed on the conductive layer. The outer substrate has an insulator layer over a semiconductor device layer. The two bonding surfaces are that of the semiconductor bonding layer and that of the insulator layer. Those elements are missing in all the examples of the cited references.

Not only do the cited references lack the elements in claim 1, neither one teaches, suggests or provides any incentive supporting the combination of the references. Furthermore, even the combination of the two references would not have taught all the elements of claim 1 of the prevent invention. Therefore, 103(b) rejection is improper based on the cited references.

2. Prior art does not teach the problem or its source.

A patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the "subject matter as a whole" which should always be considered in determining the obviousness of an invention under 35 U.S.C. §103.[3] The cited references do not teach the problem of film delamination or its source, which is the lack of a cohesive bond.

As explained in the Summary of the Invention section of the specification, an important technical advantage of the present invention inheres in the fact that the SOI architecture disclosed provides for a buried conductive layer but still provides for a cohesive bond between the buried substrate and the outer device layers associated with the bonded substrate.[4] The cohesive bond results following the process described in claim 1. The need for cohesive bond between conductive layer and the device layer is

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[2] See U.S. 6,255,731 B1, Abstract
[3] In re Zurko, 111 F.3d 887, 42 USPQ2D 1476 (Fed. Cir. 1997)
[4] Specification, page 3, ll 18-23.

not taught in the cited reference. Therefore, 103(b) rejection is improper based on the cited references.

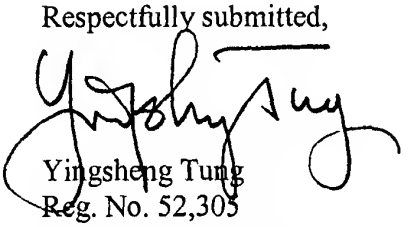
3. Not all claims limitations are considered, especially when missing form the prior art.

The mere absence from the reference of an explicit requirement of the claim cannot reasonably be construed as an affirmative statement that the requirement is in the reference.[5] At least one explicit element in claim 1 is missing in both cited references.

Kondo reference teaches bonding oxide layer to metal layer. Ohmi teaches bonding conductive layer to conductive layer. Therefore the elements of "forming a semiconductive bonding layer on an outer surface of the buried conductive layer and bonding an outer substrate to the outer surface of the bonding layer," are missing and cannot reasonably be construed as an affirmative statement that the requirement is in the reference. Therefore, 103(b) rejection is improper based on the cited references.

Applicant respectfully submits that the application is in allowable form and the claims distinguishable to the cited references. Applicant respectfully requests the allowance of claims 1-6 of this application.

Respectfully submitted,



Yingsheng Tung
Reg. No. 52,305
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-5355

[5] In re Evanega, 829 F.2d 1110, 4 USPQ2d 1249 (Fed. Cir. 1987)